

AMENDMENTS TO THE CLAIMS

Claim 1 (previously presented) A method of forming a split programming virtual ground (SPVG) SONOS memory, comprising:

- 5 providing a substrate having at least a first conductive type well positioned in the substrate, and a plurality of select gate structures arranged in parallel and positioned on the first conductive type well;
- forming a plurality of sacrificial spacers alongside each select gate structure;
- performing an implantation process by utilizing the select gate structures and the
- 10 sacrificial spacers as a mask to form a second conductive type doped region in the first conductive type well between two adjacent select gate structures;
- removing the sacrificial spacers;
- forming a composite dielectric layer covering the select gate structures subsequent to forming the second conductive type doped region in the first
- 15 conductive type well between two adjacent select gate structures; and
- forming a plurality of word lines perpendicular to the select gate structures on the composite dielectric layer.

- Claim 2 (original) The method of claim 1, wherein each select gate structure from
- 20 bottom to top comprises a gate insulating layer, a polysilicon layer, and a cap layer.

Claim 3 (original) The method of claim 1, wherein the second conductive type doped regions serve as buried bit lines.

- 25 Claim 4 (original) The method of claim 1, wherein the composite dielectric layer is an ONO tri-layer dielectric.

- Claim 5 (original) The method of claim 1, wherein the first conductive type well is a P well.

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Claim 6 (original) The method of claim 5, wherein each second conductive type doped region is an N doped region.

Claim 7 (previously presented) A method of forming a dual-bit storage nonvolatile memory, comprising:

- 5 providing a plurality of select gate structures arranged in parallel on the substrate;
- forming a sacrificial spacer alongside each select gate structure;
- performing an implantation process by utilizing the select gate structures and the sacrificial spacers as a mask to form a doped region in the substrate between any two adjacent select gate structures;
- removing the sacrificial spacers;
- 10 forming a composite dielectric layer covering the select gate structures subsequent to forming the doped region in the substrate between any two adjacent select gate structures; and
- forming a plurality of word lines perpendicular to the select gate structures on the composite dielectric layer.

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Claim 8 (original) The method of claim 7, wherein each select gate structure from bottom to top comprises a gate insulating layer and a conductive layer.

- 20 Claim 9 (previously presented) The method of claim 8, wherein the conductive layer is a polysilicon layer, and the nonvolatile memory is a split programming virtual ground (SPVG) SONOS memory.

- 25 Claim 10 (previous presented) The method of claim 8, wherein the conductive layer is a metal layer, and the nonvolatile memory is a split programming virtual ground (SPVG) MONOS memory.

Claim 11 (original) The method of claim 7, wherein each select gate structure further comprises a cap layer positioned on the conductive layer.

- 30 Claim 12 (currently amended) The method of claim 7, wherein the substrate further comprises a ~~linear~~ liner oxide layer positioned on the substrate and covering each select gate structure.

Claim 13 (original) The method of claim 7, wherein the doped regions serve as buried bit lines.

- 5 Claim 14 (original) The method of claim 7, wherein the composite dielectric layer is an ONO tri-layer dielectric.

Claim 15 (original) The method of claim 7, wherein the substrate further comprises at least a well, and the select gate structures are positioned on the well.

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Claim 16 (original) The method of claim 15, wherein the well is a P well, and each doped region is an N doped region.